Claims

1. A method of simulating an integrated circuit layout, the method comprising:
automatically identifying empty areas in a layout that can be filled; and
generating fill patterns to fill the empty areas.

2. The method of claim 1, further comprising:
automatically filling the empty spaces with the fill patterns.

3. The method of claim 1, further comprising:
selecting the fill patterns; and
placing the fill patterns in empty areas to fill the empty areas.

4. The method of claim 1, further comprising:
filling select empty areas with the fill patterns.

5. The method of claim 1, further comprising:
defining a unique layout cell for each fill pattern that is placed in a designated library.

6. The method of claim 1, further comprising:
using a configuration file to define the fill patterns.

7. The method of claim 1, wherein automatically identifying empty areas in a layout that can be filled, further comprises:
running an empty area identification design tool that is based on design rule checking (DRC) requirements.

8. The method of claim 1, further comprising:

using a hierarchical database that is adapted to provide easy modification or move-ability of fill patterns.

9. The method of claim 1, further comprising:

filling select empty areas with the fill patterns, wherein the select empty areas represent different layers of mask and metal in the integrated circuit.

10. The method of claim 9, wherein at least one of the different layers is filled with different shape fill patterns than the shapes in fill patterns of the other different layers.

11. A method of simulating an integrated circuit layout design, the method comprising:

identifying empty areas in the layout design;

representing the empty areas; and

generating fill patterns to fill the empty areas.

12. The method of claim 11, wherein the empty areas are represented as polygons.

13. The method of claim 12, further comprising:

using a recursive partition algorithm on select empty areas to partition the select empty areas into multiple rectangles to be filled with the fill patterns.

14. The method of claim 11, further comprising;

filling empty areas with the fill patterns.

15. The method of claim 14, further comprising:

running a design rule checking (DRC) test on the design.

16. The method of claim 15, further comprising:

when the design does not pass the DRC test, modifying the design layout.

17. The method of claim 15, further comprising:

when the design does not pass the DRC test, modifying the empty areas and fill patterns.

18. The method of claim 11, further comprising;

selecting one or more fill patterns; and

filling selected empty areas with select fill patterns.

19. The method of claim 18, further comprising:

running a design rule checking (DRC) test on the design.

20. The method of claim 19, further comprising:

when the design does not pass the DRC test, modifying the design layout.

21. The method of claim 19, further comprising:

when the design does not pass the DRC test, modifying the empty areas and fill patterns.

22. A machine readable medium having instructions stored thereon for simulating a layout of an integrated circuit, the machine readable medium instructions comprising:

automatically identifying empty areas in a layout that can be filled; and

generating fill patterns to fill the empty areas.

23. The machine readable medium instructions of claim 22, further comprising:

automatically filling the empty spaces with the fill patterns.

24. The machine readable medium instructions of claim 22, further comprising:

selecting the fill patterns; and

placing at least one select fill pattern in at least one empty area to fill the at least one empty area.

25. The machine readable medium instructions of claim 22, further comprising:

defining a unique layout cell for each fill pattern that is placed in a designated library.

26. The machine readable medium instructions of claim 22, further comprising:

using a configuration file to define the fill patterns.

27. The machine readable medium instructions of claim 22, wherein automatically identifying empty areas in a layout that can be filled, further comprises:

running an empty area identification design tool that is based on design rule checking (DRC) requirements.

28. The machine readable medium instructions of claim 22, further comprising:

using a hierarchical database that is adapted to provide easy modification or move-ability of fill patterns.

29. The method of claim 22, wherein the empty areas are represented as polygons.

30. The method of claim 29, further comprising:

using a recursive partition algorithm on select empty areas to partition the select empty areas into multiple rectangles to be filled with the fill patterns.

31. The method of claim 22, further comprising:

filling select empty areas with the fill patterns, wherein the select empty areas represent different layers of mask and metal in the integrated circuit.

32. The method of claim 31, wherein at least one of the different layers is filled with different shape fill patterns than the shapes in fill patterns of the other different layers.